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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Martin C. Roberts et al.	)	Examiner: Neal Berezsny
	)	
Serial No.: 09/745,780	)	Group Art Unit: 2823
	)	
Filed: December 21, 2000	)	Docket: 303.451US6
	)	
For: METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS	)	

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on July 10, 2002, from the Rejection of claims 38-45, 47-52, 54-59, 62-65 and 68-79 of the above-identified application, as set forth in the Final Office Action mailed April, 10, 2003.

This Appeal Brief is filed in triplicate and accompanied by an authorization to charge the requisite fee set forth in 37 C.F.R. § 117(f) and any extension of time fee to Appellants' deposit account 19-0743. Applicants respectfully request reversal of the Examiner's rejection of pending claims

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APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc., a Delaware corporation doing business at 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707-0006.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to the Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 38-45, 47-52, 54-59, 62-65 and 68-79 are pending and the subject of the present appeal (see Appendix I). No other claims remain in the application.

All of the claims are also subject to an obviousness double patenting rejection which Appellants do not dispute, other than observing that submission of a Terminal Disclaimer would be premature at this time, until the exact wording of the claims to be allowed is established. Once claims are allowed a Terminal Disclaimer will be filed.

4. STATUS OF AMENDMENTS

This application was originally filed on December 21, 2000, with claims 34-52 pending after entry of the Preliminary Amendment filed with the application which is a continuation of U.S. Serial Number 08/390,714 filed February 17, 1995 which remains pending.

Preliminary Amendment and Response to Restriction Requirement Office filed August 23, 2001.

Amendment and Response to Office Action filed February 22, 2002

Amendment and Response to Final Office Action filed September 5, 2002 with RCE.

Amendment and Response to first Office Action after RCE filed September 27, 2002.

Final Office Action after RCE was mailed April 10, 2003.

A Notice of Appeal was filed on July 10, 2003.

5. SUMMARY OF THE INVENTION

The invention relates to a an intermediate structure for the manufacture of a semiconductor interconnect having a via formed in a first polysilcon layer to expose a buried contact region on a substrate and a second polysilicon layer formed in the via to form and electrical interconnect.

6. ISSUES PRESENTED FOR REVIEW

Were claims 38-45, 47-52, 54-59, 62-65 and 68-79 properly rejected under 35 U.S.C. § 103?

7. GROUPING OF CLAIMS

The claims do not stand or fall together. Appellant suggests the following groups of claims which are in accord with the grouping of the claims established by the Examiner in earlier rejections. Within each group, each claim does stand or fall with the other claims in that group and any dependent claims to those claims; each group being argued separately below.

Group I: 38

Group II: 39, 40, 41 and 47

Group III: 42 and 43

Group IV: 45

Group V: 48, 49 and 50

Group VI: 51 and 52.

Appellant does not make any admission that any claim may not be argued in another forum as independently patentable from any other claim.

8. ARGUMENT

The Applicable Law

"A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a).

A determination of the obviousness or nonobviousness of claimed subject matter is a legal conclusion based on several factual inquiries. These include determining the scope and content of the prior art, ascertaining the differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere Co.,* 148 USPQ 459, 467 (1966); *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1586 (Fed. Cir. 2000).

In ascertaining the differences between the prior art and the claims, courts are required to consider the claimed invention as a whole. *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). It is impermissible to use the claimed invention as a "template" to piece together the teachings of the prior art to render the claimed invention obvious. *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). The claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit,* 1 USPQ2d at 1597. A §103 reference must also be considered in its entirety, "including portions that would lead away from the invention." *Id.* A court must consider not only the similarities, but also the "critical differences between the claimed invention and the prior art." *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

In establishing obviousness, two or more references each containing elements of the claimed invention may be combined, provided all the recited claim elements are met and that there is a suggestion, teaching or motivation to combine the references. *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Further, even if the prior art provides such a suggestion, motivation or teaching, a reasonable expectation of success for the suggested combination must be shown. *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

In the relatively recent case of *In re Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002), reiterated the prior cases and specifically required that

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching motivation or suggestion to select and combine the references relied on as evidence of obviousness" 61 USPQ2d at 1433.

The Federal Circuit in *In re Lee* also indicated that the "factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority." 61 USPQ2d at 1434.

Argument

The Examiner failed to make out a *prima facie* case of obviousness in rejecting claims 38-45, 47-52, 54-59, 62-65, and 68-79 under 35 U.S.C. § 103(a) on the Nihira et al patent. There is no teaching or suggestion to combine what is shown or suggested in that patent with the other elements of which the Examiner took "Official Notice." as being in the prior art. Even if Nihira et al is combined with other matter in the manner proposed by the Examiner, the rejection does not show all the elements of Appellant's claimed invention.

1. There is no support for Examiner's contention that a motivation to combine need not be shown where he relies upon four patents to support a rejection but still charactdesrizes the rejection as being based upon a single patent

The rejection in the Final Office Action now appealed from originally rejected all of the pending claims based solely upon the Nihira et al patent. That rejection had been previously made in a Final Office Action of December 6, 2001, another on June 5, 2002, and a non-Final Office Action after RCE on September 27, 2002. A chronology showing evolution of the rejection is pertinent to Appellant's contention that the rejection fails to state a prima facie case of obviousness.

In responding to the rejection of December 6, 2001, Appellant challenged the single patent obviousness rejection as failing to comply with the requirement that "all of the claim limitations must be taught or suggested by the prior art" citing MPEP 2143.03. That Office Action had conceded that there were differences between what was in the Nihira et al patent and the elements

of the rejected claims. The rejection proposed took "Official Notice" to account for the differences. Appellants duly traversed the assertion of "Official Notice".

The Office Action of December 6, 2001 took Official Notice that "the use of photoresist is well known in the art as a means of patterning structures in the semiconductor industry and would be obvious to form the resist, as recited, as part of a conventional multilevel interconnect process to enable formation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit".

The Office Action of December 6, 2001 also took Official Notice that "As is well known as a dopant and it would have been obvious to switch the dopant types of the structure to provide greater process and device latitude". Additionally that Office Action states: "Further, it would be obvious and is well known to use As as an N-type dopant".

The Office Action of December 6, 2001 took further Official Notice that ".... it would be obvious to employ an etch stop layer in an etch-back planarization process, as recited, as part of a conventional multilevel interconnected process to enable formulation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit." Additionally, the Office Action asserted "It is well known to employ an etch stop over a structure that one would like to protect during an etching process so as not to overetch the structure, causing it damage". Finally that Office Action further stated "...the use of Ti silicide as an etch stop material is also well known in the art and would be obvious to use in a conductive poly structure in order to both stop an etch and to further increase the conductivity of the structure."

Appellants duly traversed each and every one of the instances where the December 6 Office Action took Official Notice and requested the Examiner to provide references that describe such elements or to submit the affidavit required by 37 C.F.R. § 1.104(d)(2).

In the Office Action of June 5, 2002 the Examiner responded to the request for references by identifying patents to Schrantz et al 5,683,939 (asserted to teach " the use of photresist for patterning" and "the use of an etch stop in an etch-back planarization process"), Kosa et al 5,416,736 ("use of titanium silicide as an etch stop layer") and Shibib 5,541,429 ("arsenic is used to dope polysilicon to form a conducting material and could be switched with other dopants").

Quotes are from page 6 of Office Action of June 5, 2002.

The Examiner did not present any rationale for combining any of the three newly cited patent with the Nihira et al patent beyond the briefly quoted material above.

The three newly cited patents allegedly showing the features that the Examiner conceded were not shown in Nihira et al were nonetheless combined with Nihira et al. Although the three additional patents were not explicitly incorporated into the heading or office action summary of the 103 rejection, the final Office Action appealed from asserts "The references cited are to support examiner's assertions as to what is well known in the art..." Of course that is precisely the reason that any patent is cited in an obviousness rejection.

In response to Appellants contention that it was necessary to show evidence of a motivation to combine the elements supported by Official Notice Statements with an unsupported blanket assertion that the Official Notice Statements "contain motivational statements to modify the reference." (see page 8, lines 4-7 of Final Office Action of April 10, 2003. The Examiner then followed with the assertion that is at the core of this appeal:

> "Please note that the rejection is based on the modification of a single reference and the other cited references are used to support the examiner's assertion that such elements are well known in the art and are common knowledge to the skilled artisan. <u>There is no requirement that these references must be combined to form a multi-reference 103 rejection, especially when the single reference 103 rejection is proper.</u> (Final Office Action of April 10, 2003, page 8 lines 7-12 (emphasis added)"

Thus the Examiner contends that his providing additional patent references in response to the timely demand for substantiation of his earlier taking of "Official Notice" does not convert a single reference rejection to one based on a combination of multiple references. He overlooks the fact that references are cited in any rejection in an attempt to argue that the claimed invention is already available in the prior art.

In stating that the rejection supported by four patents remains a single patent rejection, the Examiner seeks to escape the clear requirement that a teaching from one source cannot be combined another to support an obviousness rejection without showing evidence of a motivation to combine. See *In re Sang Su Lee, supra*

Appellants respectfully submit that there is no support in the case law for the Examiner's contention that "there is no requirement that these references must be combined."

There is no difference in principle between an obviousness rejection initially supported by combining the teachings of a plurality of references and one based upon a single reference with the missing elements later supported by additional patents evidencing elements or modifications that were originally provided by the Examiner taking Official Notice.

In either case, the law requires the Examiner to show a reason to combine the subject matter relied upon to support an obviousness rejection. Failure to show such a "motivation to combine" demonstrates that the rejection is defective since Office Action has not made out a *prima facie* case of obviousness.

2. The Office Action has not shown where every element of the claims is alleged to be found in Nihira et al (or the other three patents cited to support areas where Official Notice was taken

Even if one were to contend that the Examiner provided evidence demonstrating a motivation to combine the various "teachings" of Nihira with the elements supported by Official Notice and/or supplemental patent references, the Examiner has still not provided a showing that each and every element of each claim is obvious in view of his assertion of what is in the prior art. Set forth below on a claim-by-claim basis is a listing of an exemplary element in each claim which is not described even in the Examiner's improper combination of references. While there are additional elements of the claims which are not covered by the combination proposed by the Examiner in the rejection, the showing of the exemplary examples below demonstrates that the rejection does no make a prima facie showing of obviousness and the claims are allowable.

Claim 38

Appellants respectfully submit that Nihira does not show a structure where "the second polycrystalline layer overlies the first polycrystalline layer" as claim 38 requires. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "first polysilicon layer" and el. 11 as a "second polysilicon layer," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed

by the specification, Nihira does not show or suggest a structure where the second polysilicon layer overlies the first polysilicon layer. Although the Examiner contends that it does overlie it between Figs E and 8F, the specification citation supporting the allegation refers to a different embodiment illustrated in Figure 3. The Examiner has failed to demonstrate that all elements of the claim are in the Nihira patent.

Claims 39, 40, 41, 47

Appellants also respectfully submit that Nihira does not show a structure where an etch stop layer is "overlying the first polycrystalline silicon layer" and there is a second polycrystalline silicon layer which is "overlying the etch stop layer and the first substrate region as claims 39, 40, require. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "first polysilicon layer" and el. 11 as a "second polysilicon layer," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where the second polysilicon layer overlies an etch stop layer and the first substrate region as claims 39 and 40 require.

Claims 42 and 43

Appellants also respectfully submit that Nihira does not show a structure where there is a photoresist mask "overlying the first polycrystalline silicon plug" and there is a polycrystalline silicon plug which is "overlying the first substrate region" as claims 42 and 43, require. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "polysilicon layer" and el. 11 as the "polysilicon plug," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where a photoresist mask overlies the first polysilicon plug an the polysilicon plug overlies a first substrate region as claims 42 and 43 require.

The Examiner, in the Final Office Action, did not attempt to rebut this assertion which was made in an earlier amendment was not

Claim 45

Appellants also respectfully submit that Nihira does not show a structure where a polycrystalline silicon plug is "overlying the first substrate region" as claim 45 requires. There is no polysilicon plug in Nihira et al. There are films 9 and 11. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where a polycrystalline silicon plug overlies the first substrate region as claim 45 requires.

Claims 48, 49, 50

Applicant understands that the Office Action relies upon element. 9 of Nihira as the "first polysilicon layer" and el. 11 as the polysilicon plug, allegedly as shown in Fig. 8f (except 11 is a film, not a plug). As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where the etch stop layer overlies the first substrate region. It does not show one where a polysilicon plug overlies the first substrate region as claims 48, 49 and 50 require.

Claims 51 and 52

Appellants also respectfully submit that Nihira does not show a structure where an etch stop layer is "overlying the polycrystalline silicon plug" and there is a polycrystalline silicon plug which is "overlying the first substrate region" as claims 51 and 52 require. Applicant understands that the Office Action relies upon el. 9 of Nihira as the "first polysilicon layer" and el. 11 as the polycrystalline silicon plug as shown in Fig. 8f (note that el. 11 is a film not a plug). As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where an etch stop layer overlies a polycrystalline silicon plug and the polycrystalline silicon plug overlies first substrate region as claim 51 requires.

Dependent claims

The rejection of each of the dependent claims is unsustainable for the same reasons as explained for the parent independent claims.

3. Conclusion

The rejection which is at the heart of this appeal is defective since it has not shown a motivation for combining the various elements taken from the prior art to support the rejection. Even if there were a showing that the references relied upon could be combined, the Final Office Action has not shown how such a combination would cover all elements of each of the claims. Reconsideration and withdrawal of the rejection and allowance of all of the pending claims is respectfully requested.

9. SUMMARY

For the foregoing reasons, the Appellant respectfully submits that the rejection of claims 38-45, 47-52, 54-59, 62-65, and 68-79 under 35 U.S.C. § 103(a) was erroneous. Reversal of those rejections is respectfully requested, as well as the allowance of all the claims.

Please charge Deposit Account 19-0743 to cover the fee required to file the Brief..

Respectfully submitted,

Martin C. Roberts et al

By their Representatives,

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Date October 10, 2003

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 20231, on this 10th day of October, 2003.

Amy Moriarty
Name

_____
Signature

APPENDIX

The Claims on Appeal

38. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region; and

a second polycrystalline silicon layer overlying the first polycrystalline silicon layer and the first substrate region.

39. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

41. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide regions;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

44. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the [field oxide and gate] oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

45. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

46. (Previously Canceled)

47. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

48. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first

polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer

and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

53. (Previously Presented) The intermediate of claim 38 wherein the first substrate region includes a buried contact region.

54. (Previously Presented)The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. (Previously Presented) The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

56. (Previously Presented) The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. (Previously Presented) The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. (Previously Presented) The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

59. (Previously Presented) The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.

60. (Previously Presented) The intermediate of claim 42 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

61. (Previously Presented) The intermediate of claim 43 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

62. (Previously Presented) The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

63. (Previously Presented) The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

64. (Previously Presented) The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

65. (Previously Presented) The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.

66. - 67. (Canceled)

68. (Previously Presented) The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

69. (Previously Presented) The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

70. (Previously Presented) The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. (Previously Presented) The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. (Previously Presented) The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. (Previously Presented) The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. (Previously Presented) The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. (Previously Presented) The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. (Previously Presented) The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. (Previously Presented) The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

78. (Previously Presented) The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. The intermediate of claim 78 wherein the first polycrystalline silicon layer and the

79. (Previously Presented) The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

APPENDIX II

Cited Statutes, Rules, and Case law

I. Statutes and Rules

- 35 U.S.C. § 103(a)

II. Case law

- *Graham v. John Deere Co.,* 148 USPQ 459, 467 (1966).
- *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1586 (Fed. Cir. 2000).
- *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987).
- *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992).
- *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).
- *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).
- *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).
- *In re Lee,* 61 USPQ2d 143 (Fed Cir. 2002)

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U.S. PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Martin C. Roberts et al.	)	Examiner: Neal Berezsny
	)	
Serial No.: 09/745,780	)	Group Art Unit: 2823
	)	
Filed: December 21, 2000	)	Docket: 303.451US6
	)	
For: METHOD FOR FORMING AN INTEGRATED CIR-CUIT INTERCONNECT USING A DUAL POLY PROCESS	)	

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on July 10, 2002, from the Rejection of claims 38-45, 47-52, 54-59, 62-65 and 68-79 of the above-identified application, as set forth in the Final Office Action mailed April, 10, 2003.

This Appeal Brief is filed in triplicate and accompanied by an authorization to charge the requisite fee set forth in 37 C.F.R. § 117(f) and any extension of time fee to Appellants' deposit account 19-0743. Applicants respectfully request reversal of the Examiner's rejection of pending claims

APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc., a Delaware corporation doing business at 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707-0006.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to the Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 38-45, 47-52, 54-59, 62-65 and 68-79 are pending and the subject of the present appeal (see Appendix I). No other claims remain in the application.

All of the claims are also subject to an obviousness double patenting rejection which Appellants do not dispute, other than observing that submission of a Terminal Disclaimer would be premature at this time, until the exact wording of the claims to be allowed is established. Once claims are allowed a Terminal Disclaimer will be filed.

4. STATUS OF AMENDMENTS

This application was originally filed on December 21, 2000, with claims 34-52 pending after entry of the Preliminary Amendment filed with the application which is a continuation of U.S. Serial Number 08/390,714 filed February 17, 1995 which remains pending.

Preliminary Amendment and Response to Restriction Requirement Office filed August 23, 2001.

Amendment and Response to Office Action filed February 22, 2002

Amendment and Response to Final Office Action filed September 5, 2002 with RCE.

Amendment and Response to first Office Action after RCE filed September 27, 2002.

Final Office Action after RCE was mailed April 10, 2003.

A Notice of Appeal was filed on July 10, 2003.

5. SUMMARY OF THE INVENTION

The invention relates to a an intermediate structure for the manufacture of a semiconductor interconnect having a via formed in a first polysilcon layer to expose a buried contact region on a substrate and a second polysilicon layer formed in the via to form and electrical interconnect.

6. ISSUES PRESENTED FOR REVIEW

Were claims 38-45, 47-52, 54-59, 62-65 and 68-79 properly rejected under 35 U.S.C. § 103?

7. GROUPING OF CLAIMS

The claims do not stand or fall together. Appellant suggests the following groups of claims which are in accord with the grouping of the claims established by the Examiner in earlier rejections. Within each group, each claim does stand or fall with the other claims in that group and any dependent claims to those claims; each group being argued separately below.

Group I: 38

Group II: 39, 40, 41 and 47

Group III: 42 and 43

Group IV: 45

Group V: 48, 49 and 50

Group VI: 51 and 52.

Appellant does not make any admission that any claim may not be argued in another forum as independently patentable from any other claim.

8. ARGUMENT

The Applicable Law

"A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a).

A determination of the obviousness or nonobviousness of claimed subject matter is a legal conclusion based on several factual inquiries. These include determining the scope and content of the prior art, ascertaining the differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere Co.,* 148 USPQ 459, 467 (1966); *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1586 (Fed. Cir. 2000).

In ascertaining the differences between the prior art and the claims, courts are required to consider the claimed invention as a whole. *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). It is impermissible to use the claimed invention as a "template" to piece together the teachings of the prior art to render the claimed invention obvious. *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). The claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit,* 1 USPQ2d at 1597. A §103 reference must also be considered in its entirety, "including portions that would lead away from the invention." *Id.* A court must consider not only the similarities, but also the "critical differences between the claimed invention and the prior art." *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

In establishing obviousness, two or more references each containing elements of the claimed invention may be combined, provided all the recited claim elements are met and that there is a suggestion, teaching or motivation to combine the references. *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Further, even if the prior art provides such a suggestion, motivation or teaching, a reasonable expectation of success for the suggested combination must be shown. *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

In the relatively recent case of *In re Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002), reiterated the prior cases and specifically required that

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching motivation or suggestion to select and combine the references relied on as evidence of obviousness" 61 USPQ2d at 1433.

The Federal Circuit in *In re Lee* also indicated that the "factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority." 61 USPQ2d at 1434.

Argument

The Examiner failed to make out a *prima facie* case of obviousness in rejecting claims 38-45, 47-52, 54-59, 62-65, and 68-79 under 35 U.S.C. § 103(a) on the Nihira et al patent. There is no teaching or suggestion to combine what is shown or suggested in that patent with the other elements of which the Examiner took "Official Notice." as being in the prior art. Even if Nihira et al is combined with other matter in the manner proposed by the Examiner, the rejection does not show all the elements of Appellant's claimed invention.

1. There is no support for Examiner's contention that a motivation to combine need not be shown where he relies upon four patents to support a rejection but still charactdesrizes the rejection as being based upon a single patent

The rejection in the Final Office Action now appealed from originally rejected all of the pending claims based solely upon the Nihira et al patent. That rejection had been previously made in a Final Office Action of December 6, 2001, another on June 5, 2002, and a non-Final Office Action after RCE on September 27, 2002. A chronology showing evolution of the rejection is pertinent to Appellant's contention that the rejection fails to state a prima facie case of obviousness.

In responding to the rejection of December 6, 2001, Appellant challenged the single patent obviousness rejection as failing to comply with the requirement that "all of the claim limitations must be taught or suggested by the prior art" citing MPEP 2143.03. That Office Action had conceded that there were differences between what was in the Nihira et al patent and the elements

of the rejected claims. The rejection proposed took "Official Notice" to account for the differences. Appellants duly traversed the assertion of "Official Notice".

The Office Action of December 6, 2001 took Official Notice that "the use of photoresist is well known in the art as a means of patterning structures in the semiconductor industry and would be obvious to form the resist, as recited, as part of a conventional multilevel interconnect process to enable formation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit".

The Office Action of December 6, 2001 also took Official Notice that "As is well known as a dopant and it would have been obvious to switch the dopant types of the structure to provide greater process and device latitude". Additionally that Office Action states: "Further, it would be obvious and is well known to use As as an N-type dopant".

The Office Action of December 6, 2001 took further Official Notice that ".... it would be obvious to employ an etch stop layer in an etch-back planarization process, as recited, as part of a conventional multilevel interconnected process to enable formulation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit." Additionally, the Office Action asserted "It is well known to employ an etch stop over a structure that one would like to protect during an etching process so as not to overetch the structure, causing it damage". Finally that Office Action further stated "...the use of Ti silicide as an etch stop material is also well known in the art and would be obvious to use in a conductive poly structure in order to both stop an etch and to further increase the conductivity of the structure."

Appellants duly traversed each and every one of the instances where the December 6 Office Action took Official Notice and requested the Examiner to provide references that describe such elements or to submit the affidavit required by 37 C.F.R. § 1.104(d)(2).

In the Office Action of June 5, 2002 the Examiner responded to the request for references by identifying patents to Schrantz et al 5,683,939 (asserted to teach " the use of photresist for patterning" and "the use of an etch stop in an etch-back planarization process"), Kosa et al 5,416,736 ("use of titanium silicide as an etch stop layer") and Shibib 5,541,429 ("arsenic is used to dope polysilicon to form a conducting material and could be switched with other dopants").

Quotes are from page 6 of Office Action of June 5, 2002.

The Examiner did not present any rationale for combining any of the three newly cited patent with the Nihira et al patent beyond the briefly quoted material above.

The three newly cited patents allegedly showing the features that the Examiner conceded were not shown in Nihira et al were nonetheless combined with Nihira et al. Although the three additional patents were not explicitly incorporated into the heading or office action summary of the 103 rejection, the final Office Action appealed from asserts "The references cited are to support examiner's assertions as to what is well known in the art..." Of course that is precisely the reason that any patent is cited in an obviousness rejection.

In response to Appellants contention that it was necessary to show evidence of a motivation to combine the elements supported by Official Notice Statements with an unsupported blanket assertion that the Official Notice Statements "contain motivational statements to modify the reference." (see page 8, lines 4-7 of Final Office Action of April 10, 2003. The Examiner then followed with the assertion that is at the core of this appeal:

> "Please note that the rejection is based on the modification of a single reference and the other cited references are used to support the examiner's assertion that such elements are well known in the art and are common knowledge to the skilled artisan. <u>There is no requirement that these references must be combined to form a multi-reference 103 rejection, especially when the single reference 103 rejection is proper.</u> (Final Office Action of April 10, 2003, page 8 lines 7-12 (emphasis added)"

Thus the Examiner contends that his providing additional patent references in response to the timely demand for substantiation of his earlier taking of "Official Notice" does not convert a single reference rejection to one based on a combination of multiple references. He overlooks the fact that references are cited in any rejection in an attempt to argue that the claimed invention is already available in the prior art.

In stating that the rejection supported by four patents remains a single patent rejection, the Examiner seeks to escape the clear requirement that a teaching from one source cannot be combined another to support an obviousness rejection without showing evidence of a motivation to combine. See *In re Sang Su Lee, supra*

Appellants respectfully submit that there is no support in the case law for the Examiner's contention that "there is no requirement that these references must be combined."

There is no difference in principle between an obviousness rejection initially supported by combining the teachings of a plurality of references and one based upon a single reference with the missing elements later supported by additional patents evidencing elements or modifications that were originally provided by the Examiner taking Official Notice.

In either case, the law requires the Examiner to show a reason to combine the subject matter relied upon to support an obviousness rejection. Failure to show such a "motivation to combine" demonstrates that the rejection is defective since Office Action has not made out a *prima facie* case of obviousness.

2. The Office Action has not shown where every element of the claims is alleged to be found in Nihira et al (or the other three patents cited to support areas where Official Notice was taken

Even if one were to contend that the Examiner provided evidence demonstrating a motivation to combine the various "teachings" of Nihira with the elements supported by Official Notice and/or supplemental patent references, the Examiner has still not provided a showing that each and every element of each claim is obvious in view of his assertion of what is in the prior art. Set forth below on a claim-by-claim basis is a listing of an exemplary element in each claim which is not described even in the Examiner's improper combination of references. While there are additional elements of the claims which are not covered by the combination proposed by the Examiner in the rejection, the showing of the exemplary examples below demonstrates that the rejection does no make a prima facie showing of obviousness and the claims are allowable.

Claim 38

Appellants respectfully submit that Nihira does not show a structure where "the second polycrystalline layer overlies the first polycrystalline layer" as claim 38 requires. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "first polysilicon layer" and el. 11 as a "second polysilicon layer," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed

by the specification, Nihira does not show or suggest a structure where the second polysilicon layer overlies the first polysilicon layer. Although the Examiner contends that it does overlie it between Figs E and 8F, the specification citation supporting the allegation refers to a different embodiment illustrated in Figure 3. The Examiner has failed to demonstrate that all elements of the claim are in the Nihira patent.

Claims 39, 40, 41, 47

Appellants also respectfully submit that Nihira does not show a structure where an etch stop layer is "overlying the first polycrystalline silicon layer" and there is a second polycrystalline silicon layer which is "overlying the etch stop layer and the first substrate region as claims 39, 40, require. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "first polysilicon layer" and el. 11 as a "second polysilicon layer," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where the second polysilicon layer overlies an etch stop layer and the first substrate region as claims 39 and 40 require.

Claims 42 and 43

Appellants also respectfully submit that Nihira does not show a structure where there is a photoresist mask "overlying the first polycrystalline silicon plug" and there is a polycrystalline silicon plug which is "overlying the first substrate region" as claims 42 and 43, require. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "polysilicon layer" and el. 11 as the "polysilicon plug," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where a photoresist mask overlies the first polysilicon plug an the polysilicon plug overlies a first substrate region as claims 42 and 43 require.

The Examiner, in the Final Office Action, did not attempt to rebut this assertion which was made in an earlier amendment was not

Claim 45

Appellants also respectfully submit that Nihira does not show a structure where a polycrystalline silicon plug is "overlying the first substrate region" as claim 45 requires. There is no polysilicon plug in Nihira et al. There are films 9 and 11. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where a polycrystalline silicon plug overlies the first substrate region as claim 45 requires.

Claims 48, 49, 50

Applicant understands that the Office Action relies upon element. 9 of Nihira as the "first polysilicon layer" and el. 11 as the polysilicon plug, allegedly as shown in Fig. 8f (except 11 is a film, not a plug). As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where the etch stop layer overlies the first substrate region. It does not show one where a polysilicon plug overlies the first substrate region as claims 48, 49 and 50 require.

Claims 51 and 52

Appellants also respectfully submit that Nihira does not show a structure where an etch stop layer is "overlying the polycrystalline silicon plug" and there is a polycrystalline silicon plug which is "overlying the first substrate region" as claims 51 and 52 require. Applicant understands that the Office Action relies upon el. 9 of Nihira as the "first polysilicon layer" and el. 11 as the polycrystalline silicon plug as shown in Fig. 8f (note that el. 11 is a film not a plug). As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where an etch stop layer overlies a polycrystalline silicon plug and the polycrystalline silicon plug overlies first substrate region as claim 51 requires.

Dependent claims

The rejection of each of the dependent claims is unsustainable for the same reasons as explained for the parent independent claims.

3. Conclusion

The rejection which is at the heart of this appeal is defective since it has not shown a motivation for combining the various elements taken from the prior art to support the rejection. Even if there were a showing that the references relied upon could be combined, the Final Office Action has not shown how such a combination would cover all elements of each of the claims. Reconsideration and withdrawal of the rejection and allowance of all of the pending claims is respectfully requested.

9. SUMMARY

For the foregoing reasons, the Appellant respectfully submits that the rejection of claims 38-45, 47-52, 54-59, 62-65, and 68-79 under 35 U.S.C. § 103(a) was erroneous. Reversal of those rejections is respectfully requested, as well as the allowance of all the claims.

Please charge Deposit Account 19-0743 to cover the fee required to file the Brief..

Respectfully submitted,

Martin C. Roberts et al

By their Representatives,

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Date October 10, 2003

By _____
Charles E. Steffey
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 20231, on this 10th day of October, 2003.

Amy Moriarty
Name

_____
Signature

APPENDIX

The Claims on Appeal

38. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region; and

a second polycrystalline silicon layer overlying the first polycrystalline silicon layer and the first substrate region.

39. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

41. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide regions;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

44. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the [field oxide and gate] oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

45. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

46. (Previously Canceled)

47. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

48. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first

polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer

and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

53. (Previously Presented) The intermediate of claim 38 wherein the first substrate region includes a buried contact region.

54. (Previously Presented)The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. (Previously Presented) The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

56. (Previously Presented) The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. (Previously Presented) The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. (Previously Presented) The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

59. (Previously Presented) The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.

60. (Previously Presented) The intermediate of claim 42 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

61. (Previously Presented) The intermediate of claim 43 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

62. (Previously Presented) The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

63. (Previously Presented) The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

64. (Previously Presented) The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

65. (Previously Presented) The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.

66. - 67. (Canceled)

68. (Previously Presented) The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

69. (Previously Presented) The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

70. (Previously Presented) The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. (Previously Presented) The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. (Previously Presented) The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. (Previously Presented) The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. (Previously Presented) The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. (Previously Presented) The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. (Previously Presented) The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. (Previously Presented) The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

78. (Previously Presented) The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. The intermediate of claim 78 wherein the first polycrystalline silicon layer and the

79. (Previously Presented) The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

APPENDIX II

Cited Statutes, Rules, and Case law

I. Statutes and Rules

- 35 U.S.C. § 103(a)

II. Case law

- *Graham v. John Deere Co.,* 148 USPQ 459, 467 (1966).
- *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1586 (Fed. Cir. 2000).
- *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987).
- *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992).
- *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).
- *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).
- *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).
- *In re Lee,* 61 USPQ2d 143 (Fed Cir. 2002)

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OCT 14 2003
U.S. PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Martin C. Roberts et al.	)	Examiner: Neal Berezsny
	)	
Serial No.: 09/745,780	)	Group Art Unit: 2823
	)	
Filed: December 21, 2000	)	Docket: 303.451US6
	)	
For: METHOD FOR FORMING AN INTEGRATED CIR-CUIT INTERCONNECT USING A DUAL POLY PROCESS	)	

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on July 10, 2002, from the Rejection of claims 38-45, 47-52, 54-59, 62-65 and 68-79 of the above-identified application, as set forth in the Final Office Action mailed April, 10, 2003.

This Appeal Brief is filed in triplicate and accompanied by an authorization to charge the requisite fee set forth in 37 C.F.R. § 117(f) and any extension of time fee to Appellants' deposit account 19-0743. Applicants respectfully request reversal of the Examiner's rejection of pending claims

APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc., a Delaware corporation doing business at 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707-0006.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to the Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 38-45, 47-52, 54-59, 62-65 and 68-79 are pending and the subject of the present appeal (see Appendix I). No other claims remain in the application.

All of the claims are also subject to an obviousness double patenting rejection which Appellants do not dispute, other than observing that submission of a Terminal Disclaimer would be premature at this time, until the exact wording of the claims to be allowed is established. Once claims are allowed a Terminal Disclaimer will be filed.

4. STATUS OF AMENDMENTS

This application was originally filed on December 21, 2000, with claims 34-52 pending after entry of the Preliminary Amendment filed with the application which is a continuation of U.S. Serial Number 08/390,714 filed February 17, 1995 which remains pending.

Preliminary Amendment and Response to Restriction Requirement Office filed August 23, 2001.

Amendment and Response to Office Action filed February 22, 2002

Amendment and Response to Final Office Action filed September 5, 2002 with RCE.

Amendment and Response to first Office Action after RCE filed September 27, 2002.

Final Office Action after RCE was mailed April 10, 2003.

A Notice of Appeal was filed on July 10, 2003.

5. SUMMARY OF THE INVENTION

The invention relates to a an intermediate structure for the manufacture of a semiconductor interconnect having a via formed in a first polysilcon layer to expose a buried contact region on a substrate and a second polysilicon layer formed in the via to form and electrical interconnect.

6. ISSUES PRESENTED FOR REVIEW

Were claims 38-45, 47-52, 54-59, 62-65 and 68-79 properly rejected under 35 U.S.C. § 103?

7. GROUPING OF CLAIMS

The claims do not stand or fall together. Appellant suggests the following groups of claims which are in accord with the grouping of the claims established by the Examiner in earlier rejections. Within each group, each claim does stand or fall with the other claims in that group and any dependent claims to those claims; each group being argued separately below.

Group I: 38

Group II: 39, 40, 41 and 47

Group III: 42 and 43

Group IV: 45

Group V: 48, 49 and 50

Group VI: 51 and 52.

Appellant does not make any admission that any claim may not be argued in another forum as independently patentable from any other claim.

8. ARGUMENT

The Applicable Law

"A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a).

A determination of the obviousness or nonobviousness of claimed subject matter is a legal conclusion based on several factual inquiries. These include determining the scope and content of the prior art, ascertaining the differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere Co.,* 148 USPQ 459, 467 (1966); *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1586 (Fed. Cir. 2000).

In ascertaining the differences between the prior art and the claims, courts are required to consider the claimed invention as a whole. *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). It is impermissible to use the claimed invention as a "template" to piece together the teachings of the prior art to render the claimed invention obvious. *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). The claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit,* 1 USPQ2d at 1597. A §103 reference must also be considered in its entirety, "including portions that would lead away from the invention." *Id.* A court must consider not only the similarities, but also the "critical differences between the claimed invention and the prior art." *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

In establishing obviousness, two or more references each containing elements of the claimed invention may be combined, provided all the recited claim elements are met and that there is a suggestion, teaching or motivation to combine the references. *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Further, even if the prior art provides such a suggestion, motivation or teaching, a reasonable expectation of success for the suggested combination must be shown. *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

In the relatively recent case of *In re Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002), reiterated the prior cases and specifically required that

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching motivation or suggestion to select and combine the references relied on as evidence of obviousness" 61 USPQ2d at 1433.

The Federal Circuit in *In re Lee* also indicated that the "factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority." 61 USPQ2d at 1434.

Argument

The Examiner failed to make out a *prima facie* case of obviousness in rejecting claims 38-45, 47-52, 54-59, 62-65, and 68-79 under 35 U.S.C. § 103(a) on the Nihira et al patent. There is no teaching or suggestion to combine what is shown or suggested in that patent with the other elements of which the Examiner took "Official Notice." as being in the prior art. Even if Nihira et al is combined with other matter in the manner proposed by the Examiner, the rejection does not show all the elements of Appellant's claimed invention.

1. There is no support for Examiner's contention that a motivation to combine need not be shown where he relies upon four patents to support a rejection but still charactdesrizes the rejection as being based upon a single patent

The rejection in the Final Office Action now appealed from originally rejected all of the pending claims based solely upon the Nihira et al patent. That rejection had been previously made in a Final Office Action of December 6, 2001, another on June 5, 2002, and a non-Final Office Action after RCE on September 27, 2002. A chronology showing evolution of the rejection is pertinent to Appellant's contention that the rejection fails to state a prima facie case of obviousness.

In responding to the rejection of December 6, 2001, Appellant challenged the single patent obviousness rejection as failing to comply with the requirement that "all of the claim limitations must be taught or suggested by the prior art" citing MPEP 2143.03. That Office Action had conceded that there were differences between what was in the Nihira et al patent and the elements

of the rejected claims. The rejection proposed took "Official Notice" to account for the differences. Appellants duly traversed the assertion of "Official Notice".

The Office Action of December 6, 2001 took Official Notice that "the use of photoresist is well known in the art as a means of patterning structures in the semiconductor industry and would be obvious to form the resist, as recited, as part of a conventional multilevel interconnect process to enable formation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit".

The Office Action of December 6, 2001 also took Official Notice that "As is well known as a dopant and it would have been obvious to switch the dopant types of the structure to provide greater process and device latitude". Additionally that Office Action states: "Further, it would be obvious and is well known to use As as an N-type dopant".

The Office Action of December 6, 2001 took further Official Notice that ".... it would be obvious to employ an etch stop layer in an etch-back planarization process, as recited, as part of a conventional multilevel interconnected process to enable formulation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit." Additionally, the Office Action asserted "It is well known to employ an etch stop over a structure that one would like to protect during an etching process so as not to overetch the structure, causing it damage". Finally that Office Action further stated "...the use of Ti silicide as an etch stop material is also well known in the art and would be obvious to use in a conductive poly structure in order to both stop an etch and to further increase the conductivity of the structure."

Appellants duly traversed each and every one of the instances where the December 6 Office Action took Official Notice and requested the Examiner to provide references that describe such elements or to submit the affidavit required by 37 C.F.R. § 1.104(d)(2).

In the Office Action of June 5, 2002 the Examiner responded to the request for references by identifying patents to Schrantz et al 5,683,939 (asserted to teach " the use of photresist for patterning" and "the use of an etch stop in an etch-back planarization process"), Kosa et al 5,416,736 ("use of titanium silicide as an etch stop layer") and Shibib 5,541,429 ("arsenic is used to dope polysilicon to form a conducting material and could be switched with other dopants").

Quotes are from page 6 of Office Action of June 5, 2002.

The Examiner did not present any rationale for combining any of the three newly cited patent with the Nihira et al patent beyond the briefly quoted material above.

The three newly cited patents allegedly showing the features that the Examiner conceded were not shown in Nihira et al were nonetheless combined with Nihira et al. Although the three additional patents were not explicitly incorporated into the heading or office action summary of the 103 rejection, the final Office Action appealed from asserts "The references cited are to support examiner's assertions as to what is well known in the art..." Of course that is precisely the reason that any patent is cited in an obviousness rejection.

In response to Appellants contention that it was necessary to show evidence of a motivation to combine the elements supported by Official Notice Statements with an unsupported blanket assertion that the Official Notice Statements "contain motivational statements to modify the reference." (see page 8, lines 4-7 of Final Office Action of April 10, 2003. The Examiner then followed with the assertion that is at the core of this appeal:

> "Please note that the rejection is based on the modification of a single reference and the other cited references are used to support the examiner's assertion that such elements are well known in the art and are common knowledge to the skilled artisan. <u>There is no requirement that these references must be combined to form a multi-reference 103 rejection, especially when the single reference 103 rejection is proper.</u> (Final Office Action of April 10, 2003, page 8 lines 7-12 (emphasis added)"

Thus the Examiner contends that his providing additional patent references in response to the timely demand for substantiation of his earlier taking of "Official Notice" does not convert a single reference rejection to one based on a combination of multiple references. He overlooks the fact that references are cited in any rejection in an attempt to argue that the claimed invention is already available in the prior art.

In stating that the rejection supported by four patents remains a single patent rejection, the Examiner seeks to escape the clear requirement that a teaching from one source cannot be combined another to support an obviousness rejection without showing evidence of a motivation to combine. See *In re Sang Su Lee, supra*

Appellants respectfully submit that there is no support in the case law for the Examiner's contention that "there is no requirement that these references must be combined."

There is no difference in principle between an obviousness rejection initially supported by combining the teachings of a plurality of references and one based upon a single reference with the missing elements later supported by additional patents evidencing elements or modifications that were originally provided by the Examiner taking Official Notice.

In either case, the law requires the Examiner to show a reason to combine the subject matter relied upon to support an obviousness rejection. Failure to show such a "motivation to combine" demonstrates that the rejection is defective since Office Action has not made out a *prima facie* case of obviousness.

2. The Office Action has not shown where every element of the claims is alleged to be found in Nihira et al (or the other three patents cited to support areas where Official Notice was taken

Even if one were to contend that the Examiner provided evidence demonstrating a motivation to combine the various "teachings" of Nihira with the elements supported by Official Notice and/or supplemental patent references, the Examiner has still not provided a showing that each and every element of each claim is obvious in view of his assertion of what is in the prior art. Set forth below on a claim-by-claim basis is a listing of an exemplary element in each claim which is not described even in the Examiner's improper combination of references. While there are additional elements of the claims which are not covered by the combination proposed by the Examiner in the rejection, the showing of the exemplary examples below demonstrates that the rejection does no make a prima facie showing of obviousness and the claims are allowable.

Claim 38

Appellants respectfully submit that Nihira does not show a structure where "the second polycrystalline layer overlies the first polycrystalline layer" as claim 38 requires. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "first polysilicon layer" and el. 11 as a "second polysilicon layer," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed

by the specification, Nihira does not show or suggest a structure where the second polysilicon layer overlies the first polysilicon layer. Although the Examiner contends that it does overlie it between Figs E and 8F, the specification citation supporting the allegation refers to a different embodiment illustrated in Figure 3. The Examiner has failed to demonstrate that all elements of the claim are in the Nihira patent.

Claims 39, 40, 41, 47

Appellants also respectfully submit that Nihira does not show a structure where an etch stop layer is "overlying the first polycrystalline silicon layer" and there is a second polycrystalline silicon layer which is "overlying the etch stop layer and the first substrate region as claims 39, 40, require. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "first polysilicon layer" and el. 11 as a "second polysilicon layer," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where the second polysilicon layer overlies an etch stop layer and the first substrate region as claims 39 and 40 require.

Claims 42 and 43

Appellants also respectfully submit that Nihira does not show a structure where there is a photoresist mask "overlying the first polycrystalline silicon plug" and there is a polycrystalline silicon plug which is "overlying the first substrate region" as claims 42 and 43, require. Applicant understands that the Office Action relies upon el. 9 of Nihira as a "polysilicon layer" and el. 11 as the "polysilicon plug," as shown in Fig. 8f. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where a photoresist mask overlies the first polysilicon plug an the polysilicon plug overlies a first substrate region as claims 42 and 43 require.

The Examiner, in the Final Office Action, did not attempt to rebut this assertion which was made in an earlier amendment was not

Claim 45

Appellants also respectfully submit that Nihira does not show a structure where a polycrystalline silicon plug is "overlying the first substrate region" as claim 45 requires. There is no polysilicon plug in Nihira et al. There are films 9 and 11. As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where a polycrystalline silicon plug overlies the first substrate region as claim 45 requires.

Claims 48, 49, 50

Applicant understands that the Office Action relies upon element. 9 of Nihira as the "first polysilicon layer" and el. 11 as the polysilicon plug, allegedly as shown in Fig. 8f (except 11 is a film, not a plug). As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where the etch stop layer overlies the first substrate region. It does not show one where a polysilicon plug overlies the first substrate region as claims 48, 49 and 50 require.

Claims 51 and 52

Appellants also respectfully submit that Nihira does not show a structure where an etch stop layer is "overlying the polycrystalline silicon plug" and there is a polycrystalline silicon plug which is "overlying the first substrate region" as claims 51 and 52 require. Applicant understands that the Office Action relies upon el. 9 of Nihira as the "first polysilicon layer" and el. 11 as the polycrystalline silicon plug as shown in Fig. 8f (note that el. 11 is a film not a plug). As can be seen in Figure 8f and confirmed by the specification, Nihira does not show or suggest a structure where an etch stop layer overlies a polycrystalline silicon plug and the polycrystalline silicon plug overlies first substrate region as claim 51 requires.

Dependent claims

The rejection of each of the dependent claims is unsustainable for the same reasons as explained for the parent independent claims.

3. Conclusion

The rejection which is at the heart of this appeal is defective since it has not shown a motivation for combining the various elements taken from the prior art to support the rejection. Even if there were a showing that the references relied upon could be combined, the Final Office Action has not shown how such a combination would cover all elements of each of the claims. Reconsideration and withdrawal of the rejection and allowance of all of the pending claims is respectfully requested.

9. SUMMARY

For the foregoing reasons, the Appellant respectfully submits that the rejection of claims 38-45, 47-52, 54-59, 62-65, and 68-79 under 35 U.S.C. § 103(a) was erroneous. Reversal of those rejections is respectfully requested, as well as the allowance of all the claims.

Please charge Deposit Account 19-0743 to cover the fee required to file the Brief..

Respectfully submitted,

Martin C. Roberts et al

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Date October 10, 2003

By _____
Charles E. Steffey
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 20231, on this 10th day of October, 2003.

Amy Moriarty
Name

_____
Signature

APPENDIX

The Claims on Appeal

38. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region; and

a second polycrystalline silicon layer overlying the first polycrystalline silicon layer and the first substrate region.

39. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

41. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide regions;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

44. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the [field oxide and gate] oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

45. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

46. (Previously Canceled)

47. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

48. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first

polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer

and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

53. (Previously Presented) The intermediate of claim 38 wherein the first substrate region includes a buried contact region.

54. (Previously Presented)The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. (Previously Presented) The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

56. (Previously Presented) The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. (Previously Presented) The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. (Previously Presented) The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

59. (Previously Presented) The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.

60. (Previously Presented) The intermediate of claim 42 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

61. (Previously Presented) The intermediate of claim 43 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

62. (Previously Presented) The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

63. (Previously Presented) The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

64. (Previously Presented) The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

65. (Previously Presented) The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.

66. - 67. (Canceled)

68. (Previously Presented) The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

69. (Previously Presented) The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

70. (Previously Presented) The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. (Previously Presented) The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. (Previously Presented) The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. (Previously Presented) The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. (Previously Presented) The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. (Previously Presented) The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. (Previously Presented) The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. (Previously Presented) The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

78. (Previously Presented) The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. The intermediate of claim 78 wherein the first polycrystalline silicon layer and the

79. (Previously Presented) The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

APPENDIX II

Cited Statutes, Rules, and Case law

I. Statutes and Rules

- 35 U.S.C. § 103(a)

II. Case law

- *Graham v. John Deere Co.,* 148 USPQ 459, 467 (1966).
- *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1586 (Fed. Cir. 2000).
- *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987).
- *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992).
- *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).
- *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).
- *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).
- *In re Lee,* 61 USPQ2d 143 (Fed Cir. 2002)